

IN THE DRAWINGS

Fig. 1 has been amended, as illustrated in the red-lined and replacement drawing.

REMARKS

Claims 1 – 3, 5 – 13, and 15 – 26 are pending. Claims 4 and 14 have been cancelled. Claims 1, 6, 7, 11, and 16 – 19 have been amended. Claims 22 - 26 have been added. No new matter has been added. Reexamination and reconsideration of this application are respectfully requested.

In the August 9, 2005 Office Action, the Examiner stated that Fig. 1 should be labeled as prior art. The applicants have included replacement sheets labeling Fig. 1 and Fig. 2 as prior art in order to address the Examiner's concerns.

In the August 9, 2005 Office Action, the Examiner stated that claims 1 – 21 were rejected under 35 U.S.C. § 112, second paragraph as being indefinite. The Examiner stated that there appears to be a contradiction in the estimating step because how could estimating an error become a corrected value. The applicants have amended the claims to address the Examiner's concern. Specifically, the limitation has been changed to recited "estimating an error of the value of the input signal, amplifying the error of the value to create an amplified error, and holding the amplified error of the value as a corrected value to be utilized if the tentative value is to be corrected." The error value, after amplification, may be utilized as a corrected value if the tentative value is to be corrected.

The Examiner also noted that claims 1, 6, 11, and 19 recited "the correcting of the tentative value to the corrected value" and that this was not clear. The applicants have amended claims 1, 6, 11, and 19 to recite that the corrected value is selected instead of the tentative value if the two recited conditions are met. Accordingly, applicants respectfully submit that the Examiner's rejection of claims 1 – 21 under 35

U.S.C. § 112, second paragraph should be withdrawn.

The Examiner also stated that claims 7 and 15 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants have rewritten claim 7 to include all of the limitations of the base claim and any intervening claim. Applicants have rewritten claim 15 to include some of the limitations of the base claim and intervening claims. In claim 15, applicants have deleted duplicative limitations and also deleted additional limitations describing features of the receiver. Applicants still believe claim 15 is in condition for allowance because the applicants have included the limitation the Examiner stated are not taught by the prior art, i.e, **that a error verifier module including an absolute value circuit and comparator** is not taught by the prior art. Accordingly, applicants respectfully submit that claims 7 and 15 are in condition for allowance. Dependent claim 23 recites limitations similar to claims 7 and 15 and applicants respectfully submit that claim 23 is also in condition for allowance.

The Examiner rejected claims 1 – 6, 8 - 10, and 19 - 21 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Published Patent Application 2001/0016926 to Riggle (“the Riggle reference”) in view of U.S. Patent No. 6,084,931 to Powell (“the Powell reference”). The Examiner rejected claims 11 – 14 and 16 under 35 U.S.C. § 103(a) as being unpatentable over the Riggle reference in view of the Powell reference and further in view of U.S. Patent No. 6,556,637 to Moriuchi (“the Moriuchi reference”). The Examiner rejected claims 17 and 18 under 35 U.S.C. § 103(a) as being unpatentable over the Riggle reference in view of the Powell reference and the Moriuchi reference and further in view of U.S. Patent No. 6,549,604 to Shenoi (“the Shenoi

reference.) These rejections are respectfully traversed in so far as it is applicable to the presently pending claims.

Independent claim 1, as amended, distinguishes over the cited references.
Claim 1 recites:

A method of error correction in a high-speed data transmission system, comprising:
determining a value of an input signal at a decision timeframe and holding the value as a tentative value;
estimating an error of the value of the input signal by subtracting the tentative value from the value of the input signal, amplifying the error of the value to create an amplified error, and holding the amplified error of the value as a corrected value to be utilized if the tentative value is to be corrected;
deciding if the amplified error of the value is within a defined marginal range;
determining if the input signal is involved in a transition from a positive to negative state or from a negative to positive state during a symbol period; and
selecting the corrected value instead of the tentative value to be output if both the amplified error of the value is in the defined marginal range and the input signal is involved in the transition.

The Riggle reference does not disclose, teach, or suggest the method of error correction as recited claim 1, as amended. The Examiner states that the Riggle reference discloses an error estimator module (15, 56) to determine an error value, to amplify the error value, and to hold the amplified error value as a corrected value. The Examiner specifically states that in paragraph 41 an inverter has the opposite bit from the bit output from data decision circuit 16. (*Office Action, page 4*). Specifically, the Riggle reference discloses that a first decision unit 15 produces a detected signal that is available at an output of the DFE unit 36 and is called the primary bit string. An inverter 56 is operative for receiving the primary bit string inverting the bits of the bit string to create an inverted bit string. The multiplexer 58 is operative for changing a secondary

bit string by allowing, for each bit time, the present bit of the primary bit string, the inverted bit string or detected signal of second decision unit 16 to pass it to an input port. (*Riggle, paragraph 41*).

This is the not the same as a method of error correction including **estimating an error of the value of the input signal by subtracting the tentative value from the value of the input signal, amplifying the error of the value to create an amplified error, and holding the amplified error of the value as a corrected value to be utilized if the tentative value is to be corrected**, as is recited in claim 1, as amended.

The Riggle reference does not disclose estimating an error of the value of the input signal by subtracting the tentative value from the value of the input signal and by amplifying the error of the value to create an amplified error. Instead, the Riggle reference discloses that a primary bit string is detected at the first decision unit and then an inverter 56 creates an inverted bit string. In addition, sampled data is input a forward FIR equalizer 12, where the forward FIR equalizer 12 processes the data samples according to a predetermined filter response function to create modified data samples. The modified data samples are then sent to a subtractor 14 which further modifies the data samples by subtracting feedback values from the data samples to create modified data samples S. The data samples are then fed to the decision unit which supplies a very simple detection algorithm. (*Riggle, paragraph 31*). There is no disclosure in the Riggle reference that an **error of the value is created by subtracting the value of the input signal and then amplifying the error of the value**. Instead, the Riggle reference is directed to either detecting an input signal, creating an inverted signal from input signal, or subtracting feedback values from the data samples to create

modified data samples. The Riggle reference never discloses that a tentative value is subtracted from the input signal and then is amplified because in the Riggle reference a feedback value is subtracted from an input signal, but then that value is fed to a decision unit. In addition, there is no disclosure of **amplification** in the Riggle reference. Accordingly, applicants respectfully submit that claim 1, as amended, distinguishes over the Riggle reference.

In addition, the Riggle reference does not disclose a method of error correction in a high-speed data transmission system, including **selecting the corrected value instead of the tentative value to be output if both the amplified error of the value is in the defined marginal range and the input signal is involved in the transition.** The Riggle reference discloses only that a multiplexer 58 is operative to create a secondary bit string by allowing one of the present bit of the primary bit string, the inverted bit string, or the detected signal of a second decision unit to pass to an output port. A control unit makes the decision on which to select based upon a low signal flag. A comparator 52 receives the input data samples and compares the magnitude of the samples to a first threshold value to create a low signal flag. (*Riggle, paragraph 41*).

There is no disclosure in the Riggle reference that **a corrected value is selected if both the amplified error of the value is in the defined marginal range and the input signal is involved in the transition.** The Riggle reference makes a determination to select one of the primary bit string and the inverted bit string signals depending on the value of the low signal flag. The low signal flag is indicative of the magnitude of a data sample being input into the first decision unit and is related to the probability that the first decision unit will make a correct decision using the data sample.

Specifically, the multiplexer 58 passes the present bit of the primary bit string when the low signal flag is logical zero and at the time when the low signal flag becomes a logical one, the multiplexer passes the inverted bit from the primary bit string. In addition, for a selectable period of time, the multiplexer passes bits from the second decision unit 16 (in other words there is no condition). (*Riggle, paragraph 41*). The Riggle reference is not disclosing that two conditions are being checked before selecting a corrected value instead of the tentative value. Instead, the Riggle reference is disclosing a signal may be compared to a threshold value and that this may determine if a regular bit or an inverted bit is selected. The selection of a bit/inverted bit is predicated on whether an input data sample (which has been modified by both a FIR equalizer and a first feedback filter) is less than a threshold. This is not determining whether **an amplified value is within a marginal range**. Also, the inverted bit is not the same as an **amplified error value** (the corrected value). In addition, the Riggle reference also allows a selectable time where a user can select that bits from the second decision unit are utilized, which is not dependent on a condition at all. According, applicant respectfully submits that claim 1, as amended, further distinguishes over the Riggle reference.

The Powell reference does not make up for the deficiencies of the Riggle reference. The Examiner utilizes the Powell reference to disclose the limitation of “determining if the input signal is involved in a transition from a positive to negative state or from a negative to positive state during a symbol period.” (*Office Action, page 4*). Assuming, *arguendo*, that the Powell reference discloses all that the Examiner states that it does, the Power reference does not disclose a method of error correction

in a high speed data transmission system including **estimating an error of the value of the input signal by subtracting the tentative value from the value of the input signal, amplifying the error of the value to create an amplified error, and holding the amplified error of the value as a corrected value to be utilized if the tentative value is to be corrected and also selecting the corrected value instead of the tentative value to be output if both the amplified error of the value is in the defined marginal range and the input signal is involved in the transition.**

Accordingly, applicants respectfully submit that claim 1, as amended, distinguishes over the Powell / Riggle combination.

The Moriuchi and Shenoi references do not make up for the deficiencies of the Riggle and Powell references. The Examiner utilizes the Moriuchi reference to disclose a timing recovery PLL circuit providing a stable clock (*Office Action, page 7*) and utilizes the Shenoi reference to disclose a receiver receiving a T1 signal and providing a clock recovery and discovery of phase transients. (*Office Action, page 8*). Assuming, *arguendo*, that the Moriuchi and Shenoi references disclose all that the Examiner states that they do, these references do not disclose a method of error correction in a high speed data transmission system including **estimating an error of the value of the input signal by subtracting the tentative value from the value of the input signal, amplifying the error of the value to create an amplified error, and holding the amplified error of the value as a corrected value to be utilized if the tentative value is to be corrected and also selecting the corrected value instead of the tentative value to be output if both the amplified error of the value is in the defined marginal range and the input signal is involved in the transition.**

Accordingly, applicants respectfully submit that claim 1, as amended, distinguishes over the Powell / Riggle / Moriuchi / Shenoi combination.

Independent claims 6, 11, and 19, all as amended, recite limitations similar to claim 1, as amended. Accordingly applicants respectfully submit that claims 6, 11, and 19 distinguish over the Riggle / Powell / Moriuchi / Shenoi combination for reasons similar to those discussed above in regard to claim 1, as amended.

Claims 2, 3, 5, 8 – 10, 12, 13, 15 – 18, and 20 - 26 depend, directly or indirectly on claims 1, 6, 11, and 19. Accordingly, applicants respectfully submit that claims 2, 3, 5, 8 – 10, 12, 13, 15 – 18, and 20 - 26 distinguish over the Riggle / Powell / Moriuchi / Shenoi combination for the same reason as those discussed above in regard to claims 1, 6, 11, and 19.

Claim 10 distinguishes over the cited Riggle and Powell references. Claim 10 recites:

The decision system according to claim 8, wherein the transition detecting module **includes an adder to add the adjacent sample values, an absolute value circuit to make positive the added adjacent sample values, and a comparator to compare the added adjacent sample values to a reference value.**

The Riggle reference does not disclose the highlighted limitation. The Examiner states that the Riggle reference does not explicitly teach a transition detecting module. (*Office Action, page 4*). Accordingly, applicants respectfully submit that claim 10 distinguishes over the Riggle reference.

The Powell reference does not make up for the deficiencies of the Riggle reference. The Examiner states that the Powell reference discloses an adder 246, 248 to add the adjacent sample values, an absolute value circuit 224 to make positive the

added adjacent sample values, and a comparator 226, 228, and 230 to compare the added adjacent sample values to a reference value. (*Office Action, page 5*). The applicants disagree with the Examiner. The Powell reference specifically discloses (in Fig. 6, not Fig. 8 as cited by the Examiner) that adjacent samples are subtracted from each other. The Powell reference discloses that a summer 222 receives the first sample value and subtracts from it the third sample value to compute as output a difference. Then, the magnitude generation 224 outputs the absolute value or magnitude of the difference. (*Powell, col. 6, lines 26 – 33*). In other words, the Powell reference does not disclose **adding the adjacent sample values**, as is recited in claim 10. In contrast, the Powell reference discloses subtracting the sample values. Accordingly, applicants respectfully submit that claim 10 further distinguishes over the Powell / Riggle combination.

Claim 16 recites limitations similar to claim 10. Accordingly, applicants respectfully submit that claim 16 further distinguishes over the Powell / Riggle combination for reasons similar to those discussed above in regard to claim 10.

Claim 22 further distinguishes over the cited references. Claim 22 recites:

The method of claim 1, wherein **amplifying the error of the value to create an amplified error includes sending the error of the value through a signed Boolean circuit to amplify all negative values to -1 and to amplify all positive values to +1.**

None of the cited references disclose the highlighted limitation. The Riggle reference discloses that an inverter is operative for receiving the primary bit string and for inverting the bits of the bit string to create an inverted bit string (where the inverter changes logical ones to zeros and logical zeros to ones). (*Riggle, paragraph 41*).

However, this is not the same as amplifying all negative values to -1 and all positive values to +1, as is recited in claim 22. The Riggle reference is only disclosing operating on logical ones or zeros and not on operating on an error value (which could be a decimal value). Accordingly, applicants respectfully submit that claim 22 distinguishes over the Riggle / Powell / Moriuchi / Shenoi combination.

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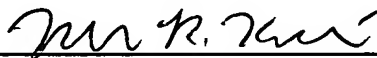
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Applicants believe that the foregoing amendments place the application in condition for allowance, and a favorable action is respectfully requested. If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call either of the undersigned attorneys at the Los Angeles telephone number (213) 488-7100 to discuss the steps necessary for placing the application in condition for allowance should the Examiner believe that such a telephone conference would advance prosecution of the application.

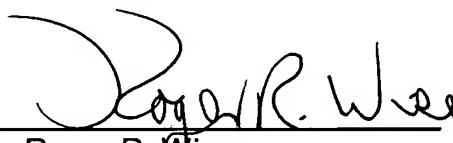
Respectfully submitted,

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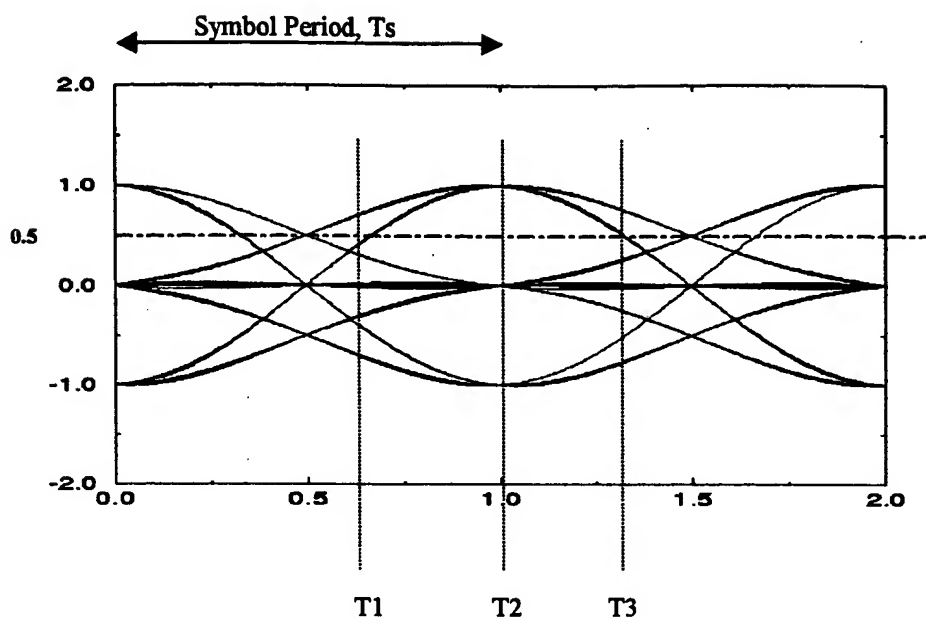


Figure 1. Eye Pattern

Prior Art